CLAIMS

1. A process for forming a barrier film to prevent poisoning a photoresist material used in forming a semiconductor device, comprising:

depositing a first barrier layer containing silicon carbide and nitrogen on a surface located to control electrical leakage from a conductor;

depositing a nitrogen-free second barrier layer on top of the first barrier layer;

forming a first low-k dielectric layer over the second barrier layer; and

depositing a photoresist material to form a photoresist layer above at least a portion of the first low-k dielectric layer.

2. The process of claim 1, further comprising patterning, and etching the photoresist layer to form a photoresist mask.

3. The process of claim 1, wherein depositing a nitrogen-free second barrier layer on top of the first barrier layer comprises depositing a nitrogen-free silicon carbide layer.

4. The process of claim 3, wherein the process tool used to deposit the first barrier layer is used to deposit the nitrogen-free second barrier layer.

5. The process of claim 1, wherein depositing a first barrier layer containing silicon carbide and nitrogen comprises using a PECVD process and one of NH_3, N_2, and N_2O as a chemical precursor to supply the nitrogen.

6. The process of claim 5, wherein depositing a nitrogen-free second barrier layer comprises using the PECVD process recited in claim 5 and turning off the supply of nitrogen.

7. The process of claim 3, further comprising:

prior to depositing said photoresist material, forming an etch stop layer on top of the second barrier layer and forming a second low-k dielectric layer on top of the etch stop layer;

patterning the photoresist layer to form a photoresist mask over a dielectric layer where a via is to be formed;

forming the via by etching through the second low-k dielectric layer, the etch stop layer, and the first low-k dielectric layer using the photoresist mask;

removing the photoresist mask;

forming and patterning a second photoresist layer to form a second photoresist mask over the second low-k dielectric layer where a trench is to be formed; and

forming a trench in the second low-k dielectric layer by etching using the second photoresist mask to complete a dual damascene structure.

8. The process of claim 7, wherein the nitrogen-free silicon carbide barrier layer is formed by injecting an $SiH_x(CH_3)_y$ gas, where x is chosen in the range of 1 to 4, and $x+y=4$.

9. The process of claim 3, further comprising:

prior to depositing said photoresist material, forming an etch stop layer on top of the second barrier layer and forming a second low-k dielectric layer on top of the etch stop layer;

patterning the photoresist layer to form a photoresist mask over the second low-k dielectric layer where a trench is to be formed;

forming the trench in the second low-k dielectric layer by etching using the photoresist mask;

forming and patterning a second photoresist layer to form a second photoresist mask over the second dielectric layer and the trench; and

forming a via in the first dielectric layer by etching to complete a dual damascene structure.

10. The process of claim 9, wherein the nitrogen-free silicon carbide barrier layer is formed by injecting an $SiH_x(CH_3)_y$ gas, where x is chosen in the range of 1 to 4, and $x+y=4$.

11. The process of claim 9, wherein depositing a first barrier layer containing silicon carbide and nitrogen comprises using a PECVD process and one of NH_3, N_2, and N_2O as a chemical precursor to supply the nitrogen.

12. The process of claim 3, further comprising:

prior to depositing said photoresist material, forming an etch stop layer on top of the second barrier layer

patterning the photoresist layer to form a photoresist mask over the etch stop layer where a via is to be formed;

forming a via mask by etching through the etch stop layer;

removing the photoresist mask;

depositing a second low-k dielectric layer on top of the via mask;

forming and patterning a second photoresist layer to form a second photoresist mask over the second low-k dielectric layer where a trench is to be formed; and

forming a trench and via by etching through the second and first low-k dielectric layers in one process step to complete a dual damascene structure.

13. The process of claim 12, wherein depositing a first barrier layer containing silicon carbide and nitrogen comprises using a PECVD process and one of NH_3, N_2, and N_2O as a chemical precursor to supply the nitrogen.

14. The process of claim 12, wherein the nitrogen-free silicon carbide barrier layer is formed by injecting an $SiH_x(CH_3)_y$ gas, where x is chosen in the range of 1 to 4, and $x+y = 4$.

15. A dual damascene semiconductor device structure comprising:

a first barrier layer containing silicon carbide and nitrogen on a surface located to control electrical leakage from a conductor;

a nitrogen-free second barrier layer on top of the first barrier layer;

a first low-k dielectric layer over the second barrier layer;

an etch stop layer deposited on top of the second barrier layer;

a second low-k dielectric layer deposited on top of the etch stop layer;

a via formed through the first low-k dielectric layer; and

a trench formed through the second low-k dielectric layer.

16. The dual damascene semiconductor device structure of claim 15 wherein the nitrogen-free second barrier layer on top of the first barrier layer comprises a nitrogen-free silicon carbide layer.

17. The dual damascene semiconductor device structure of claim 15 wherein a first barrier layer containing silicon carbide and nitrogen is deposited using a PECVD process and one of NH_3, N_2, and N_2O as a chemical precursor to supply the nitrogen

and a nitrogen-free second barrier layer is formed by turning off the supply of nitrogen.

18. The dual damascene semiconductor device structure of claim 15 wherein the nitrogen-free silicon carbide barrier layer is formed by injecting an $SiH_x(CH_3)_y$ gas, where x is chosen in the range of 1 to 4, and x+y = 4.

19. The dual damascene semiconductor device structure of claim 15 further comprising copper deposited in the trench and the via.

20. The dual damascene semiconductor device structure of claim 19 wherein the copper is deposited by an electrochemical process to fill the via and the trench.